Biographical Sketch: Sanjukta Bhanja

Executive Associate Dean, College of Engineering,
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Education

- PhD, Computer Science and Engineering, University of South Florida, 2002.
- MSC (Eng.), Electrical Engineering, Indian Institute of Science, India, 1994.
- BE, Electrical Engineering, Jadavpur University, Kolkata, 1991.

Work Experience

- 2021- till date Executive Associate Dean, College of Engineering, University of South Florida, Tampa.
- 2017-2021 Associate Dean for Academics and Student Affairs, College of Engineering, University of South Florida, Tampa.
- 2016- till date Professor, Department of Electrical Engineering, University of South Florida, Tampa.
- 2009-2016 Associate Professor, Department of Electrical Engineering, University of South Florida, Tampa.
- 2002-2008: Assistant Professor, Department of Electrical Engineering, University of South Florida, Tampa.

Honors

- Selected and certified as 2020-2021 Executive Leadership Fellow in Academic Technology, Engineering and Science (ELATES at Drexel®) program.

- Since 2002, graduated 12 PhD students, 12 MS students. Out of 12 PhD, five are from under-represented and minorities (URM) background. Most of the students are placed in High Tech Semiconductor Industries.
- Our article on magnetic non-Boolean computing got accepted to be published in Nature Nanotechnology (Impact factor 34-highest for the journals in Nanotechnology area), 2015.
- Outstanding Thesis and Dissertation Award, "Auxiliary Roles in STT-MRAM Memory", by Jayita Das, Advisor Sanjukta Bhanja, 2014-2015.
- (Student Team "Secret"-by Jayita Das, Kevin Scott, Advisor- Sanjukta Bhanja)-1st place Winner of Embedded Hardware Security Challenge, CSAW, NYU, 2014
- NSF CAREER Award 2007-2014.
- Honorable Mentions, Outstanding Graduate Faculty Mentor, University of South Florida, 2013.
- Outstanding Thesis and Dissertation Award, "Field-Coupled Nano-Magnetic Logic Systems", by Javier Pulecio, Advisor Sanjukta Bhanja, 2010-2011.
- Outstanding Undergraduate Teaching Award, University of South Florida, 2010.
- William R. Jones Outstanding Mentor Awards, Florida Education Foundation, 2010.
- Outstanding Faculty Research Achievement Award, University of South Florida, 2008.
- Outstanding Engineering Faculty Researcher, USF Tau Beta Pi, 2007.
- Honorable Mention Paper Award, IEEE International Conference on VLSI Design, 2006.
- New Researcher Award, University of South Florida, Spring 2003.
- Junior Research Fellowship, Indian Institute of Science, Bangalore, 1991-1994.
- Certificate of Merit Award, West Bengal Government, India, 1985.

Institutional and Administrative Leadership

While I document the leadership activities in this section, please note that many initiatives here are inherently collaborative in nature and are accomplished by active participation and buy-in from faculty, department chairs, associate deans, deans, and upper administration. Indeed, these are group initiatives, and I am thankful to have received overwhelming support for most of the following activities.

As **Executive Associate Dean** (2021- till date)

In this role, I am Dean's designee and responsible for the following thrusts.

1. Fiscal aspect of the College: We plan to change the budget planning, analysis, and forecasting process with transparency to all stakeholders. With the help of new team (Director of Financial Service) and tracking mechanism, we are able to provide quarterly and monthly feedback to various stakeholders, such as Department Chairs, Associate Deans, Director of Student Services. As a first step, the base-budget of the academic programs are changed from a historic value to current expenditures and commitments. Another important task will be to create a transparent budget allocation model. This work will be performed in conjunction with the Data analysis team.
2. Data Unit: While Engineering had data analysis performed at different levels before, we felt the need for an integrated data unit monitoring and forecasting admission, enrollment, graduation, research productivity, research awards, and research space utilization. This unit was established in fall 2021 and they interface closely with Finance unit and Facilities unit.
3. Space and Facilities: College is experiencing space shortage. We plan to employ two-prong approach: (1) To petition University space advisory council to get unoccupied space (especially after COVID, some units are operating fully remotely helping other units). In FY'22, College has negotiated a few new spaces by this process. (2) To use analytics and explore if we can have better model for space utilization.
4. Human Resource: HR previously used to report to financial unit. To avoid unnecessary delays, the reporting structure is completely changed. HR now directly report to EAD/Dean's designee. This has streamlined processes and eliminated red-tape signature requirements.
5. Faculty affairs: (recruitment, enrichment, tenure, and promotion): In this role, I am the Dean's designee for faculty hiring.
    - For FY'23, I am responsible for hiring eleven tenure-track faculty (three are women). Two of them have already received prestigious NSF CAREER award.
    - I have overseen mid-tenure, tenure and promotion of several faculty in Fy'22.
    - We are creating multiple College level faculty enrichment activities (with other Ads) including onboarding workshops, workshops on educational research, broader impact, and research speed-mentoring events.

6. Oversee support services (both academic and non-academic) as dean's designee. In this role, I oversee College's technical Support Service, Resource Management, Nanotechnology Research and Education center, and Facilities.
7. I have led multiple Cost-Recovery stackable certificates and degree programs in collaboration with innovative education.
8. I started and led the ABET process for BS in Cybersecurity and BS in Biomedical Engineering, this role transitioned to ADAA.
9. Represented the College of Engineering in University's strategic planning live document.

As **Associate Dean for Academic Affairs** (2017-2021)

- Co-Founder Academy of Distinguished Engineering Educator ADE^2: As an Associate Dean, I co-founded (with Dean Bishop) a faculty academy of exceptional educators. The team of five members was selected by the founders to start the Academy. Academy hosts workshops for junior faculty, gets involved in academic policy, evaluates College-wide Teaching awards, and conducts external individual and College-level educational research.
- General Education reform: The University has recently undergone general education reform. The College of Engineering went through a massive gen-ed transformation which helped us create space for technical electives. For a few high-demand programs, where course-offerings could not cope up with student demands, it helped in student progression and time to degree.
- COVID-19 and doctoral students: Led multiple assistantship and scholarship programs for doctoral students who are affected by COVID-19. In particular, international students who were not able to attend in Fall 2020 due to visa processing, we created initiatives and strategies to remove barriers to progression.
- Assessment: My unit is in-charge of ABET undergraduate assessment and Southern Association of Colleges and Schools Commission on Colleges (SACSCOC) assessment for both, undergraduate and graduate programs. We are currently going through the ABET review of seven of our academic programs.
- Summer Early-start: College of Engineering has launched a preparatory Math course to help students perform better for summer admits, whose profile suggests lack of Math preparation in high schools. This program is coupled with content-based learning teams that students

must be a part of. While our second-year retention has improved several points over the last 5 years, this program's goal is to provide a smooth social and academic boost to students who need it most.

- Engineering Communication interweaved: we have added Engineering communication to our curriculum as a vertically integrated process. For example, students learn to communicate in the Engineering domain right from the beginning in the foundation Lab. This training gets reinforced midway through the curriculum in College-wide courses such as Probability and Statistics and Engineering Economics. Students have a summative experience at upper level either in capstone or a project-based course as summative experience. We hired two Engineering communication faculty to include writing in our technical courses. They have a PhD in Communication but have worked in high tech and health science industries.
- Foundation lab: Established a College-wide First-year design experience for engineering students. All BS programs had to send faculty to teach sections of this team-taught, tightly synchronized course, which is run with the help of the Director of First-Year Experiences. I oversee the need of the course in terms of TA support (centralized and managed by the director) and hardware/software resources. Also, I am part of the design of the curriculum and learning outcome for this course.
- Admission: Created new admission criteria with the help of University Admissions to consider high school GPA as an alternate to Test Scores. This initiative will start in Fall 2020. As we know, standardized testing might adversely impact students with schools with low infrastructure.
- Recruitment Initiatives: The College of Engineering has been relying on university-level recruitment efforts. However, we have started a targeted recruitment initiative and engineering awareness campaign. We have a bi-modal focus: one towards women and URM students, and the other towards high-achieving students.
- NAE Grand Challenges Scholars Program (GCSP): Director and Founder of GCSP; In 2018, we got selected into the GCSP program established by the National Academy of Engineering (NAE). This is a three-year vertically integrated co-curricular program for the USF Engineering students.
- Diversity pledge: College of Engineering has received a Bronze recognition in 2019 to be a champion in diversity and inclusive environment. The College's effort in recruitment and

retention of URM students are seen in % of URM students being much higher than National numbers. In the next few years, our goal is to enhance strategic initiatives and partnerships to increase women in Engineering.

- Co-Led "The Pathways to Innovation Program" on behalf of Engineering. This is a training through an NSF-funded National Center for Engineering Pathways to Innovation (Epicenter), which is designed to help institutions fully incorporate innovation and entrepreneurship into undergraduate engineering education. The program is run by Epicenter, which is funded by the National Science Foundation and directed by Stanford University and the VentureWell.

Professional Leadership

- Technical program committee Architecture Track, IEEE/ACM DATE Conference 2023.
- Guest Co-editor of ACM JETC Special Issue on Advances in Design of Ultra-Low Power Circuits and Systems in Emerging Technologies, July, 2015.
- Steering Committee Member IEEE ISVLSI 2015—till date.
- Steering Committee Member ACM GLSVLSI 2010—till date.
- Member of Editorial Board IEEE Transactions on VLSI (IEEE TVLSI) 2011-2014.
- Member of Editorial Board ACM Journal on Emerging Technologies in Computing Systems (ACM JETC) 2011--.
- General Co-Chair of IEEE ISVLSI, 2014.
- General Co-Chair: "Fostering Diversity in the Design Automation for Emerging Computing Community" (Co-located workshop with DAC 2014)—2014. This is a discipline-specific Mentoring Workshop (DSW) series sponsored by the Computing Research Association's Committee on the Status of Women in Computing Research (CRAW) in an alliance with the Coalition to Diversify Computing (CDC) and the National Science Foundation.
- Steering Committee Member ACM GLSVLSI conference, 2013- till date.
- Host and General Co-Chair of National Science Foundation sponsored workshop on "Field-Coupled Nano-Computing", Held at University of South Florida campus, February, 2013.
- General Co-Chair of "1st Workshop On Design And Test Methodologies For Emerging Technologies"-- with IEEE European Test Symposium, Avignon (France), May 31, 2013.
- General Co-Chair, NanoFlorida, September 2012.
- Area Chair Emerging Technology Track, IEEE/ACM DATE Conference 2013.
- Area Co-chair Emerging Technology Track, IEEE/ACM DATE Conference 2011, 2012.
- Technical Program Committee Chair, IEEE ISVLSI Conference, 2009.
- General Co-chair ACM GLSVLSI 2009.
- Program Co-Chair IEEE/ACM Great Lake Symposium on VLSI (ACM GLSVLSI) 2008.

Departmental and University Services

- Electrical Engineering Search Committee Chair 2015.

- Member of University Graduate Council, 2014-2015
- Member of University Sabbatical Committee, 2013-2015.
- Serving in two departmental committees on personnel and academic affairs, 2010, 2011.
- Advisory Board Member for Nanotechnology Research and Education Center, USF.
- Electrical Engineering Faculty Hiring committee 2005, 2006, 2009, 2010, 2011, 2012.
- ABET subcommittee chair for Digital Analog Circuits and Embedded Systems.

Professional Services

- Track Chair-Emerging Technology Track, IEEE ISVLSI, 2019, 2020.
- Technical Program Committee, IEEE Nano, 2014-2015.
- Technical Program Committee, IEEE ISVLSI 2015.
- Technical Program Committee IEEE/ACM VLSI Design 2011, 2012.
- Technical Program Committee: IEEE DATE, 2010, IEEE/ACM VLSI Design 2010.
- Technical Program Committee of IEEE 1st Intl. Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS), 2008.
- Technical Program Committee (RCM) of IEEE International Symposium on Circuits and Systems (ISCAS) 2007, 2008.
- Technical Program Committee of ACM Great Lake Symposium on VLSI (GLSVLSI) 2007.
- Session Chair IEEE/ASEE Frontiers in Education FIE 2007.
- Session Chair ACM GLSVLSI, 2006, 2007.
- Local Arrangement Chair for IEEE symposium on VLSI 2003, 2005.
- Reviewer for Conferences IEEE/ACM DAC, IEEE VLSI Design, IEEE ISCAS, ACM GLSVLSI
- Reviewer for Journals IEEE Transactions on VLSI (TVLSI), IEEE Transactions on CAD (TCAD), IEEE Transactions on Nanotechnology (TNANO), ACM Transactions on Design Automation and Electronic Systems (TODAES).

Outreach Activities

- Member of faculty Coordinating Committee (Electrical Engineering) for Alfred P. Sloan Foundation University Centers of Exemplary Mentoring (UCEM), 2014-2019.
- Member of Florida Robotics Alliance (FRA) Board, 2013- till date.
- Sloan Director Electrical Engineering, 2011-2014.
- Invited Speaker and Mentor: "The STEM Enterprise: Beyond the Boundaries of Traditional Disciplines"- NSF funded minority student conference NC-LSAMP located at North Carolina A&T State University in Greensboro, North Carolina, September 2012.
- Host, Distinguished Lecture Series: Goal of enhancing graduate school experience for women Engineers; sponsored by *Computer Research Association's Committee on the Status of Women in Computing Research* (CRA-W), Fall 2007.
- Worked (with USF World) on Trilateral partnership with IIIT Delhi and Queen's University, Belfast (USF INTO partner), 2011-2012.
- Faculty advisor for CoE initiative for Research for High School (REHS) students (host for four students for Gaither High School in 2010-2011); Three of them are current undergraduate student at CoE.
- National Science Foundation Bridge-to-the-doctorate mentor and McKnight mentor.
- Worked with Ms. Michaela Westlake under Research Experience for Teachers (RET) program and also participating nano-education with K7, K8 students.
- Worked with Ms. Alli Pulecio with K3-K4 students on STEM outreach under Research Experience for Teachers (RET) program.
- Faculty mentor for REU students and NSF MIE program 2005.

Professional Affiliations

- Member, Association for Computing Machinery (ACM),
- Senior Member, Institute of Electrical and Electronics Engineers (IEEE),
- Member, Women in Engineering Proactive Networks (WEPAN),
- Member, American Association of University Women (AAUW).

Students Under Guidance

1. Arifa Hoque (PhD candidate)
2. Pavia Bera (PhD student)
3. Prayash Dutta (PhD student)
4. Dibyangana Kar (PhD Student)
5. Ilia A Bautista (PhD Student)

Doctoral Students Graduated

1. Kawsher Roxy (Spring 2020, Intel Corporation)
2. Ravi Panchumarthy (Fall 2015, Intel Corporation, Co-Major)
3. Sunny Kedia (Fall 2015, SRI, Co-Major)
4. Jayita Das, (Spring 2015, Intel Corporation)
5. Srinath Rajaram (2014, Micron)
6. Dinuka Karunaratne (Spring 2013, Intel Corporation)
7. Chamila Siyambalapitiyage (PhD, 2012, Intel Corporation)
8. Anita Kumari (PhD, 2011, Associate Professor, LPU, India)
9. Javier Pulecio (PhD, 2010, BNL, National Research Council Fellow at NIST, Spin Dynamics group, Currently @ IBM): Outstanding Dissertation Award 2011.
10. Karthikeyan Lingasubramanian (PhD, 2010, Assistant Professor, University of Alabama at Birmingham.
11. Saket Srivastava (PhD, 2008, Assistant Professor, Lincoln University, UK)
12. Thara Rejimon (PhD, 2006, Techgene Solutions, TX)

MS Students Graduated

Jayita Das, Srinath Rajaram, Dinuka Karunaratne, Javier Pulecio, Kevin Scott, Pruthvi Pendru, Shiva Ramani, Nirmal Ramalingam, Vivekanandan Srinivasan, Sathishkumar Ponraj, Praveen Venkataramani, Karthikeyan Lingasubramanian.

Books and Special Issues

1. K. A. Roxy and S. Bhanja, Non-Boolean Computing with Spintronic Devices. *Foundations and Trends® in Electronic Design Automation*, *12*(1), 1-123, 2018.
2. N. G. Anderson and S. Bhanja. Field-Coupled Nanocomputing: Paradigms, Progress, and Perspectives, Theoretical Computer Science and General Issues Series, *Springer*, ISBN 978-3-662-43722-3, 2014.
3. Special Issue on Advances in Design of Ultra-Low Power Circuits and Systems in Emerging Technologies, *ACM Journal of Emerging Technologies*, Editors: A. Todri-Sanial and S. Bhanja, in print 2016.

Book Chapters

1. J. Das, S. M. Alam and S. Bhanja, "STT-based Non-Volatile Logic-in-Memory Framework" in Field-Coupled Nanocomputing, edited by S. Bhanja and N. Anderson, *LNCS Series (Springer).*
2. J. Pulecio, S. Sarkar and S. Bhanja, "An Experimental Demonstration of the Viability of Energy Minimizing Computing using Nano-magnets" in "Nanoelectronic Device Applications Handbook", edited by James Morris & Krzysztof Iniewski, *CRC Press (Taylor & Francis Group)*, 2012.
3. J. Das, S. M. Alam and S. Bhanja, "Non-volatile Logic-in-Memory Architecture: An Integration between Nanomagnetic Logic and Magneto-resistive RAM" in "Nanoelectronic Device Applications Handbook", edited by James Morris & Krzysztof Iniewski, *CRC Press (Taylor & Francis Group)*, 2012.
4. S. Bhanja, M. Ottavi, S. Pontarelli and F. Lombardi, "QCA Circuits for Robust Coplanar Crossing", in "Test, Defect Tolerance and Reliability for Emerging Nanotechnologies", edited by Mohammad Tehranipoor, *Springer Science +Business Media*, LLC, 2008.
5. S. Bhanja and N. Ranganathan, "Hardware Implementation of Data Compression", in "Lossless Compression Handbook," edited by K. Saud, *Computer Society Press*, 2002.

Journal Publications

1. J. Nance, K. A. Roxy, S. Bhanja, & G. P. Carman. "Multiferroic antiferromagnetic artificial synapse." *Journal of Applied Physics* 132, no. 8 (2022): 084102.
2. S. Ollivier, S. Longofono, P. Dutta, J. Hu, S. Bhanja and A. K. Jones, "Toward Comprehensive Shifting Fault Tolerance for Domain-Wall Memories with PIETT," in *IEEE Transactions on Computers*, 2022, doi: 10.1109/TC.2022.3188206.
3. K. Roxy, S. Longofono, S. Olliver, S. Bhanja and A. K. Jones, "Pinning Fault Mode Modeling for DWM Shifting," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 7, pp. 3319-3323, July 2022, doi: 10.1109/TCSII.2022.3161594.
4. A. Hoque, A. K. Jones and S. Bhanja, "XDWM: A 2D Domain Wall Memory," in *IEEE Transactions on Nanotechnology*, vol. 21, pp. 185-188, 2022, doi: 10.1109/TNANO.2022.3158889.
5. A. Hoque A, S. Rajaram, S. Bhanja, "A Study on Reconfigurable Nanomagnetic Array and Effect of Gilbert Damping on Reconfigurability." in *IEEE Transactions on Nanotechnology*. vol. 20, pp. 503-506, 2021, doi: 10.1109/TNANO.2021.3087590.
6. K. Roxy, S. Ollivier, A. Hoque, S. Longofono, A. K. Jones and S. Bhanja, "A Novel Transverse Read Technique for Domain-Wall "Racetrack" Memories," in *IEEE Transactions on Nanotechnology*, vol. 19, pp. 648-652, 2020, doi: 10.1109/TNANO.2020.3014091.
7. J. A. Nance, K. A. Roxy, S. Bhanja and G. P. Carman, "Spin–Orbit Torque and Dipole Coupling for Nanomagnetic Array Programmability," in *IEEE Transactions on Magnetics*, vol. 56, no. 7, pp. 1-8, July 2020, Art no. 1300108, doi: 10.1109/TMAG.2020.2995514.
8. I. Bautista, S. Sarkar, S. Bhanja, "MatlabHTM: A sequence memory model of neocortical layers for anomaly detection," in SoftwareX, vol. 11, 2020, ISSN 2352-7110, https://doi.org/10.1016/j.softx.2020.100491.
9. K. A. Roxy and S. Bhanja, "Reading Nanomagnetic Energy Minimizing Coprocessor," in IEEE Transactions on Nanotechnology, vol. 17, no. 2, pp. 368-372, March 2018.
10. S. Bhanja, D.K Karunaratne, R. Panchumarthy, S. Rajaram and S. Sarkar, "Experimental Demonstration of Non-Boolean Computing in Computer Vision with Nanomagnets", in *Nature Nanotechnology (Journal Impact= 38.9)*, vol. 11, no. 2, pp.- 117—183, 2016.
11. J. Das, K. Scott, and S. Bhanja. "Mram puf: Using geometric and resistive variations in mram cells." *ACM Journal on Emerging Technologies in Computing Systems (JETC),* vol. 13, no. 1 (2016).

12. J. Das, K. Scott, S. Rajaram, D. Burgett, and S. Bhanja, "MRAM PUF: A Novel Geometry Based Magnetic PUF With Integrated CMOS", Accepted in *IEEE Transactions on Nanotechnology*, vol. 14, no. 3, pp. 436-443, 2015.
13. J. Das, S. M. Alam and S. Bhanja, "Recent Trends In Spintronics-Based Nanomagnetic Logic", *SPIN*, vol. 4, no. 3, pp. 145004, World Scientific Publishing Company, 2014.
14. J. Das, S. M. Alam and S. Bhanja, "Nano magnetic STT-logic partitioning for optimum performance", in *IEEE Transactions on Very Large Scale Integration Systems (VLSI),* vol. 22, no. 1, pp. 90-98, 2014.
15. S. Rajaram, D. K. Karunaratne, S. Sarkar, S. Bhanja, "Study of Dipolar Neighbor Interaction on Magnetization States of Nano-Magnetic Disks", in *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 3129-3132, 2013.
16. R. Panchumarthy, D.K Karunaratne, S. Sarkar, and S. Bhanja, "Magnetic State Estimator to Characterize the Magnetic States of Nano-Magnetic Disks", in *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 3545-3548, 2013.
17. J. Das, S. M. Alam and S. Bhanja, "Ultra-low Power Hybrid CMOS-Magnetic Logic Architecture", *in IEEE Transactions on Circuits and Systems I (Regular paper),* vol. 59, no. 9, pp. 2008—2016, 2012.
18. D. Karunaratne and S. Bhanja, "Study of Single Layer and Multilayer Nano-Magnetic Logic" , *Accepted in Journal of Applied Physics*, vol. 11, no. 7, pp. 07A928, 2012.
19. J. Das, S. M. Alam and S. Bhanja, "Low Power Magnetic Quantum Cellular Automata Realization Using Magnetic Multi-Layer Structures", *(Invited)* in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, pp. 267-276, 2011.
20. A. Kumari, S. Sarkar, J. Pulecio, D. Karunaratne and S. Bhanja, "Study of Magnetization State Transition in Closely-Spaced Nanomagnet 2D Array for Computation", in *Journal of Applied Physics*, vol. 109, no. 7, pp. 07E513, 2011.
21. J. Pulecio, P. Pendru, A. Kimari and S. Bhanja, "Magnetic Cellular Automata Wires", in *IEEE Transactions on Nanotechnology*, vol. 10, no. 6, pp. 1243-1248, 2011.
22. A. Kumari and S.. Bhanja, "Landauer Clocking for Magnetic Cellular Automata (MCA) Arrays", in *IEEE Transactions on VLSI Systems*, vol. 19, no. 4, pp. 714-717, 2011.
23. K. Lingasubramanian, S. Alam and S. Bhanja, "Maximum Error Modeling for Fault-Tolerant Computation using Maximum a posteriori (MAP) Hypothesis", in *Microelectronics Reliability*, pp. 485-501, ISSN "0026-2714", 2011.

24. J.Pulecio and S. Bhanja, "Magnetic Cellular Automata Coplanar Cross-wire Systems", in *Journal of Applied Physics*, vol. 107, no. 3, pp. 034308-034308-5, 2010.
25. S. Srivastava, S. Sarkar and S. Bhanja, "Power Dissipation Bounds and Models for Quantum-dot Cellular Automata Circuits", in *IEEE Transactions on Nanotechnology*, vol. 8, no. 1, pp. 116-127, 2009.
26. T. Rejimon, K. Lingasubramanian and S. Bhanja, "Probabilistic Error Model for Unreliable Nano-Logic gates" in *IEEE Transactions on VLSI Systems*, vol. 17, no. 1, pp. 55-65, 2009.
27. S. Bhanja and S. Sarkar, "Thermal Switching Error versus Delay Tradeoffs in Clocked QCA Circuits", in *IEEE Transactions on VLSI Systems*, vol. 16, no. 5, pp. 528-541, 2008.
28. S. Srivastava and S. Bhanja, "Integrating Nano-logic Knowledge Module into an Undergraduate Logic Design Course", in *IEEE Transactions on Education*, vol. 51, no. 3, pp. 349-355, 2008.
29. S. Bhanja, M. Ottavi, S. Pontarelli and F. Lombardi, "QCA Circuits for Robust Coplanar Crossing", in *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 23, no. 2, pp. 193-210, 2007.
30. S. Srivastava and S. Bhanja, "Hierarchical Probabilistic Macromodeling for QCA Circuits", in special no. of Nano Systems and Computing, *IEEE Transactions on Computers*, vol. 56, no. 2, pp. 174-190, 2007.
31. S. Bhanja and S. Sarkar, "Probabilistic Modeling of QCA Circuits using Bayesian networks", in *IEEE transaction on Nanotechnology*, vol. 5, no. 6, pp. 657-670, 2006.
32. T. Rejimon and S. Bhanja, "A Timing-Aware Probabilistic Model for Single-Event-Upset Analysis", in *IEEE Transactions on VLSI System*s, vol. 14, no. 10, pp. 1130-1139, 2006. (A preliminary version of this paper was nominated for "Best Paper Award" and received "Honorable Mention award" in *IEEE Intl. Conference of VLSI Design* 2006)
33. S. Bhanja, K. Lingasubramanian and N. Ranganathan, "A Stimulus-free Graphical Probabilistic Switching Model for Sequential Circuits using Dynamic Bayesian Networks" in *ACM Transactions on Design Automation and Electronic System*, vol. 11, no. 3, pp. 773-796, 2006.
34. T. Rejimon and S. Bhanja, "Time and Space Efficient Method for Accurate Computation of Error Detection Probabilities", in *IEE Proc. Computers & Digital Technique.*, vol. 152, no. 5, pp. 679-685, 2005.
35. S. Bhanja and N. Ranganathan, "Cascaded Bayesian Inferencing for Switching Activity Estimation with Correlated Inputs," in *IEEE Transaction on VLSI Systems*, vol. 12, no. 12, pp. 1360-1370, 2004.

36. S. Bhanja and N. Ranganathan, "Switching Activity Estimation of VLSI Circuits using Bayesian Networks," in *IEEE Transactions on VLSI Systems*, vol. 11, no. 4, pp. 558- 567, Feb. 2003.

Conference Publications (Full Paper Peer Reviewed)

1. S. Ollivier, S. Longofono, P. Dutta, J. Hu, S. Bhanja, and A. K. Jones. "CORUSCANT: Fast efficient processing-in-racetrack memories." In 2022 55th IEEE/ACM International Symposium on Microarchitecture (MICRO), pp. 784-798. IEEE, 2022.
2. Ollivier, S., Kline, D., Kawsher, R., Melhem, R., Bhanja, S., & Jones, A. K. (2019, June). "Leveraging transverse reads to correct alignment faults in domain wall memories". In *2019 49th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)* (pp. 375-387). IEEE.
3. Hoque, A., & Bhanja, S. (2018, October). "Structural Study of MgO Barrier Layer in Magnetic Devices for Computing". In 2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC) (pp. 1-4). IEEE.
4. K. A. Roxy and S. Bhanja, "Variability tolerant reading of nanomagnetic energy minimizing co-processor," 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, 2017, pp. 413-416.
5. K. A. Roxy and S. Bhanja, "Exploring the readability of nano-magnetic energy minimizing co-processor," 2017 IEEE 17th International Conference on Nanotechnology (IEEE-NANO), Pittsburgh, PA, 2017, pp. 1019-1022.
6. I. B. Adames, J. Das, and S. Bhanja. "Survey of Emerging Technology Based Physical Unclonable Functions." In *Proceedings of the 26th edition on Great Lakes Symposium on VLSI*, pp. 317-322. ACM, 2016.
7. G. Turvani, M. Bollo, J. Das, S. Bhanja, M. Graziano, M. Zamboni, , "Design of NML Circuits based on M-RAM", in *IEEE Conference on Nanotechnology*, 2015.
8. J. Das, K. Scott, D. Burgett, S. Rajaram and S. Bhanja, "A Novel Geometry Based MRAM PUF" in *IEEE Conference on Nanotechnology*, pp. 859-863, 2014.
9. J. Das, S. M. Alam, and S. Bhanja, "Prospects For Pipeline in High-Density Magnetic Field-Coupled Logic" in *IEEE Conference on Nanotechnology*, pp. 951-955, 2014.
10. R. Panchumarthy, D.K Karunaratne, S. Sarkar, and S. Bhanja, "Magnetic State Estimator to Characterize the Magnetic States of Nano-Magnetic Disks", *AIP Magnetism and Magnetic Materials Conference MMM*, 2013.

11. S. Rajaram, D. K. Karunaratne, S. Sarkar, S. Bhanja, "Study of Dipolar Neighbor Interaction on Magnetization States of Nano-Magnetic Disks", *AIP Magnetism and Magnetic Materials Conference MMM*, 2013.
12. J. Das, S. M. Alam and S. Bhanja, "Non-Destructive Variability Tolerant Differential Read for Non-Volatile Logic", in *IEEE 55th Int'l Midwest Symposium on Circuits & Systems*, pp.178-181, 2012.
13. S. Mishra and S. Bhanja, "Evaluation of Circuit Styles and VLSI Logic Designs of Pentacene OTFTs", in *IEEE 55th Int'l Midwest Symposium on Circuits & Systems*, pp. 121-124, 2012.
14. J. Das, S. M. Alam and S. Bhanja, "Addressing The Layout Constraint Problem in Cascading Logic Gates in Nanomagnetic Logic", in *IEEE Conference on Nanotechnology*, pp. 1-4, 2012.
15. J. Das, S. M. Alam and S. Bhanja, "A Novel Design Concept for High Density Hybrid CMOS-Nanomagnetic Circuits", in *IEEE Conference on Nanotechnology*, pp. 1-6, 2012.
16. S. Rajaram, D. Karunaratne and S. Bhanja, "Study of Multilayer Spintronic Devices for Logic Computation", in *IEEE INTERMAG*, 2012.
17. M. Puri and S. Bhanja, "13,6-N-sulfinylacetamidopentacene based Fully Encapsulated Low Voltage Vertical Short Channel OFET", in *OSA Solid-State and Organic Lighting (SOLED)*, November 2011.
18. J. Das, S. M. Alam, S. Rajaram and S. Bhanja, "Hybrid CMOS-MQCA Architecture using Multi-layer Spintronic Devices, WIP, IEEE/ACM Design Automation Conference (DAC), 2011.
19. D. K Karunaratne and S. Bhanja, "Programmable logic system for Magnetic Cellular Automata", in *AIP Magnetism and Magnetic Materials Conference MMM*, 2011.
20. S. Rajaram, S. Bhanja, "Boolean Logic Implementation using Coupled Spin Valves", in *AIP Magnetism and Magnetic Materials Conference MMM*, 2011.
21. J. Das, S. M. Alam and S. Bhanja, "Low Power CMOS-Magnetic Nano-Logic With Increased Bit Controllability", in *IEEE Conference on Nanotechnology*, pp. 1261-1266, 2011.
22. J. Pulecio, S. Sarkar and S. Bhanja, "Experimental Demonstration of Viability of Energy Minimizing Computing using Nano-magnets", in *IEEE Conference on Nanotechnology*, pp. 1038-1042, 2011.
23. D. Karunaratne, S. Rajaram, P. De, K. Kusmierek and S. Bhanja, "Novel knowledge module on fusion of logic and memory to undergraduate students", in *IEEE Microelectronic System Education Conference*, pp. 64-67, 2011.

24. R. Panchumarthy, D. Karunaratne, S. Sarkar and S. Bhanja, "Tool for Analysis and Quantification of Fabrication Layouts in Nanomagnet-based Computing", in *IEEE Conference on Nanotechnology*, pp. 111-115, 2011.
25. S. Bhanja and J. Pulecio, "A Review of Magnetic Cellular Automata Systems", (*Invited paper) in IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2373-2376, 2011.
26. S. Srivastava, A. Asthana, S. Bhanja and S. Sarkar "QCAPro - An Error-Power Estimation Tool for QCA Circuit Design", (*Invited paper) in IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2377-2380, 2011.
27. D. Karunaratne, J. Pulecio and S. Bhanja, "Driving Magnetic Cells for Information Storage and Propagation", in *IEEE Nanotechnology Materials and Devices Conference*, pp. 360-363, 2010.
28. A. Kumari, S. Sarkar and S. Bhanja, "Study of Magnetization State Transition in Coupled Nanomagnet for Computation", in *IEEE/AIP Magnetism and Magnetic Materials Conference MMM-Intermag*, 2010.
29. J. Pulecio and S. Bhanja, "Magnetic Cellular Automata Coplanar Cross Wire Systems", in *joint IEEE/AIP Magnetism and Magnetic Materials Conference, MMM-Intermag*, 2010.
30. J. Pulecio and S.Bhanja, "Magnetic Cellular Automata Coplanar Cross Wire Systems", in *Nano-DDS (Platform paper)*, pp. 109, 2009.
31. A. Kumari and S. Bhanja, "Magnetic Cellular Automata (MCA) Arrays under Spatially Varying Field", *(invited)* in *IEEE Nanotechnology Materials and Devices Conference*, pp. 50-53, 2009.
32. J. Pulecio and S. Bhanja, "Magnetic Cellular Automata Wires", in *IEEE Nanotechnology Materials and Devices Conference*, pp. 73-75, 2009.
33. A. Kumari, J. Pulecio and S. Bhanja, "Defect Characterization in Magnetic Field-Coupled Arrays", in *IEEE Symposium on Quality of Electronic Design*, pp. 436-441, 2009.
34. K. Lingasubramanian, S. Bhanja, "An Error Model to Study the Behavior of Transient Errors in Sequential Circuits," in *IEEE International Conference on VLSI Design*, pp. 485-490, 2009.
35. A. Shareef, K. Lingasubramanian and S. Bhanja, "Selective Redundancy: Evaluation of Temporal Reliability Enhancement Scheme for Nanoelectronic Circuits", in *IEEE Conference on Nanotechnology*, pp. 895-898, Arlington, 2008.
36. P. Venkataramani, S. Srivastava and S. Bhanja, "Sequential Circuit Design in Quantum-dot Cellular Automata", in *IEEE Conference on Nanotechnology*, pp. 534-537, Arlington, 2008.

37. S. Sarkar and S. Bhanja, "Direct Quadratic Minimization using Magnetic Field-based Computing", in *IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems*, pp. 31-34, 2008.
38. S. Srivastava, S. Sarkar and S. Bhanja, "Error-Power Tradeoffs in QCA Design", in *IEEE Conference on Nanotechnology*, pp. 530-533, Arlington, 2008.
39. J. Pulecio and S. Bhanja, "Reliability of Bi-stable Single Domain Nano Magnets for Cellular Automata", in *IEEE Conference on Nanotechnology*, pp. 782-786, Hong Kong, 2008.
40. K. Lingasubramanian and S. Bhanja, "Probabilistic Maximum Error Modeling for Unreliable Logic Circuits", in *ACM Great Lake Symposium on VLSI*, pp. 223-226, 2007.
41. S. Srivastava, S. Sarkar and S. Bhanja, "Power Dissipation Bounds and Models for Quantum-dot Cellular Automata Circuits", in *IEEE Conference on Nanotechnology*, pp. 375-378, Cincinnati, 2006.
42. S. Bhanja and S. Sarkar, "Switching Error Modes of QCA Circuits", in *IEEE Conference on Nanotechnology*, pp. 383-386, Cincinnati, 2006.
43. S. Srivastava and S. Bhanja, "Bayesian Macromodeling for Circuit Level QCA Design", in *IEEE Conference on Nanotechnology*, pp. 31-34, Cincinnati, 2006.
44. T. Rejimon and S. Bhanja, "Probabilistic Error Model for Unreliable Nano-Logic gates", in *IEEE Conference on Nanotechnology*, pp. 47-50, Cincinnati, 2006.
45. S. Bhanja, M. Ottavi, S. Pontarelli and F. Lombardi, "Novel Designs for Thermally Robust Coplanar Crossing in QCA", in *IEEE Design Automation and Test in Europe (DATE)*, vol. 1, pp. 6, 2006.
46. T. Rejimon and S. Bhanja, "A Stimulus-Free Probabilistic Model for Single-Event-Upset Sensitivity", in *IEEE International Conference on VLSI Design*, issn 1063-9667, 2006 (Nominated for "Best Paper Award" and received "Honorable mention award").
47. T. Rejimon and S. Bhanja, "Scalable Probabilistic Computing Models using Bayesian Networks", in *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 712-715, 2005.
48. V. K. Jain, S. Bhanja, G. H. Chapman, L. Doddannagari and N. Nguyen, "A Highly Reconfigurable Computing Array: DSP Plane of a 3-D Heterogeneous SoC", *IEEE SOC Conference*, pp. 243-246, 2005.
49. T. Rejimon, L. Hoffmann and S. Bhanja, "A Probabilistic Model for Single-Event-Upset", in *12th NASA Symposium on VLSI,* 2005.

50. S. Srivastava and S. Bhanja, "Hierarchical Bayesian Macromodeling for QCA Circuits", in *12th NASA Symposium on VLSI*, 2005.
51. S. Bhanja and S. Sarkar, "Graphical Probabilistic Inference for Ground State and Near-Ground State Computing in QCA Circuits", in *IEEE Nanotechnology Conference*, pp. 290-293, 2005.
52. S. Sarkar and S. Bhanja, "Synthesizing Energy Minimizing Quantum-dot Cellular Automata Circuits for Vision Computing", in *IEEE Nanotechnology Conference*, pp. 541-544, 2005.
53. N. Ramalingam and S. Bhanja, "Causal Probabilistic Input Dependency Learning for Switching Model in VLSI Circuits", in *ACM Great Lake Symposium on VLSI*, pp. 112-115, 2005.
54. S. Bhanja and S. Srivastava, "Bayesian Modeling of Quantum-dot Cellular Automata Circuits", in *Nanotech, National Science and Technology Institute*, 2005.
55. V. Jain, S. Bhanja, G. Chapman, L. Doddannagari and N. Nguyen, "A Parallel Architecture for the ICA Algorithm: DSP Plane of a 3-D Heterogeneous Sensor", in *IEEE International Conference on Acoustics, Speech, and Signal Processing*, pp. v/77- v/80, 2005.
56. T. Rejimon and S. Bhanja," An Accurate Probabilistic Model for Error Detection", in 18th *IEEE International Conference in VLSI Design*, pp.717-722, 2005.
57. S. Bhanja, K. Lingasubramanian and N. Ranganathan, "Estimation of Switching Activity in Sequential Circuits Using Dynamic Bayesian Networks," in *18th IEEE International Conference in VLSI Design*, pp. 586-591, 2005.
58. S. Ramani and S. Bhanja, "Anytime Probabilistic Switching Model using Bayesian Networks," in *IEEE International Symposium on Low Power Electronic Design*, pp. 86-89, 2004.
59. S. Bhanja and N. Ranganathan," Modeling Switching Activity Using Cascaded Bayesian Networks for Correlated Input Streams ", in *International Conference on Computer Design (ICCD)*, pp. 388-390, 2002.
60. S. Bhanja and N. Ranganathan, "Accurate Switching Activity Estimation of Large Circuits using Multiple Bayesian Networks", in *15th IEEE International Conference of VLSI Design & 7th ASP-Design and Automation Conference*, pp. 187-192, 2002.
61. S. Bhanja and N. Ranganathan, "Dependency Preserving Probabilistic Modeling of Switching Activity using Bayesian Networks," in *IEEE/ACM Design Automation Conference (DAC)*, pp. 209-214, 2001.
62. S. Bhanja, M. Fletcher-Heath, L. O. Hall, D. B. Goldgof and J. P. Krischer, "A Qualitative Expert System for Clinical Trial Assignment", in *11th International Florida Artificial Intelligence*, pp. 84-88, 1998.

Education-related Publications (Journal and Conference)

1. A. Hoque, W. Sutton, K. A. Roxy and S. Bhanja, "Integrating emerging memory technologies into undergraduate logic design course: The impact of context based teaching," 2017 IEEE International Conference on Microelectronic Systems Education (MSE), Lake Louise, AB, 2017, pp. 31-34.
2. J. Das, and S. Bhanja, "A Novel Knowledge Module to Integrate Threshold Logic and Post-CMOS Technology into Undergraduate Logic Design Classroom" in *IEEE Interdisciplinary Engineering Education Conference (IEDEC)*, pp. 24-30, March 2014.
3. C. Siyambalapitiya, R. Hyde, K. Kusmierek and S.Bhanja, "Effectiveness of Knowledge Module on "Intel 45 nm Transistor and High-k Dielectric" into Undergraduate Semiconductor Devices Course", in *IEEE 2nd Interdisciplinary Engineering Design Education Conference (IEDEC)*, pp. 83 – 87, 2011.
4. D. Karunaratne, S. Rajaram, P. De, K. Kusmierek and S. Bhanja, "Novel knowledge module on fusion of logic and memory to undergraduate students", in *IEEE Microelectronic System Education Conference*, pp. 64-67, 2011.
5. J. Pulecio, A. Pulecio, M. Westlake and S. Bhanja, "A Snapshot of Young America's Perspective towards STEM", in *IEEE Frontiers in Education (FIE)*, pp. S2E-1 – S2E-2, 2010.
6. K. Lingasubramanian and S. Bhanja, " Work In Progress - An Education Module on Engineering Ethics Concentrating on Environment-Friendly Engineering for Computer Engineers", in *IEEE Frontiers in Education (FIE)*, pp. 903-904, 2009.
7. A. Kumari and S. Bhanja, "CNT logic knowledge module integrated in digital CMOS logic design", in *IEEE Microelectronics Semiconductor Education*, pp. 115-117, 2009.
8. S. Srivastava and S. Bhanja, "Integrating Nano-logic Knowledge Module into an Undergraduate Logic Design Course", in *IEEE Transactions on Education*, vol. 51(3), pp. 349-355, 2008.
9. S. Srivastava and S. Bhanja, "WIP- Introduction of K-map based Nano-logic Synthesis in Logic Design Course", in *37th ASEE/IEEE Frontiers in Education (FIE)*, pp. S1C, 2007.
10. S. Srivastava and S. Bhanja, "Knowledge Module for Logic Design to Introduce Majority Logic Synthesis Using Karnaugh Maps", in *IEEE/ACM Intl. Conference on Microelectronic Systems Education (MSE)*, pp. 55-56, 2007.

11. S. Bhanja, "WIP: Enhancing Performance using Dominant Sensory Mode in Co-opeartive Learning Environment for VLSI Design Courses", *IEEE Frontiers in Education (FIE)*, pp. 14-15, October, 2007.

Patents

1. Das, J., Scott, K. P., Burgett, D. H., Rajaram, S., & Bhanja, S. (2020). *U.S. Patent No. 10,536,281*. Washington, DC: U.S. Patent and Trademark Office.
2. Bhansali, S., Rincon, K., Ramella-Roman, J., & Bhanja, S. (2019). *U.S. Patent No. 10,517,533*. Washington, DC: U.S. Patent and Trademark Office.
3. S. Bhanja and S. Sarkar, "Programmable Magnetic Energy Minimizing Co-processor and Method of Use", *International Provisional Patent Application No.* 1372.1073PR, filed on August 21, 2015.
4. J. Das, K. Scott, D. Burgett, S.Rajaram and S. Bhanja, "Geometry Based Magnetic PUF", *International Patent Application No.* PCT/US15/32914, filed on May 28, 2015.
5. Bhanja, S., Sarkar, S., Panchumarthy, R., & Karunaratne, D. K. (2019). *U.S. Patent No. 10,198,402*. Washington, DC: U.S. Patent and Trademark Office.

Research Funding

1. "NSF CNS 2133340: "**Collaborative Research: CNS Core: Small**: IMPERIAL: In-Memory Processing Enhanced Racetrack Inspired by Accessing Laterally", **National Science Foundation (NSF)**, PI Bhanja (USF), ($179,979.00), 2021-2024.
2. "NSF HRD/EHR 1906518: "LSAMP BD: University of South Florida Florida-Georgia Louis Stokes Alliance for Minority Participation (FGLSAMP)", **National Science Foundation (NSF)**, PI Bhanja (USF), Co-PI: Dwayne Smith, ($1,074,987.00), 2021-2022.
3. "NSF DUE 2030861 **S-STEM Track III:** "Curricular, Co-curricular, Social, and Financial Supports for Successful Transfer and Graduation of Engineering Undergraduates from Rural/Nontraditional Backgrounds", **National Science Foundation (NSF)**, PI Bhanja (USF), Co-PI : William Tyson, Reginal Webb, Bulmuo Maakuu, Mary Goodwin; ($3,070,087.00), 2020-2025.
4. "SHF: Small: Reconfigurability and Technology Integration of Magnetic Energy Minimization Co-Processor (MEMCoP)", **National Science Foundation (NSF)**, PI Bhanja (USF), Co-PI G. Carman (UCLA), ($449,999.00), 2016-2020.
5. "I-Corps: Software Suite for Quality-Control of Patterned Nanostructures", **National Science Foundation (NSF)**, PI Bhanja, ($50,000), 2014-2016.
6. "Leveraging the Radiation-Resistance and Power Efficiency of Nano-Magnetic Logic to Develop More Affordable, Efficient, and Reliable Space Technologies", **National Aeronautics & Space Administration (NASA)**, PI Bhanja, ($136,000), 2013-2015.
7. "Fostering Diversity in the Design Automation for Emerging Computing Community" (Co-located workshop with DAC 2014)—2014 Discipline-specific Mentoring Workshops (DSW) series sponsored by The Computing Research Association's Committee on the Status of Women in Computing Research (**CRAW**) in an alliance with the Coalition to Diversify Computing (**CDC**) ($20,000), Investigators: Bhanja (Lead), Hassoun, Calizo, Koomson, Harris, 2014.
8. "Fostering Diversity in the Design Automation for Emerging Computing Community" Co-sponsored by **National Science Foundation (NSF)**, PI Bhanja co-PI: Hassoun, Calizo, Koomson, Harris, ($12,000), 2014-2015.
9. Conference Supplement: Workshop on Field-Coupled Nano-computing, **National Science Foundation** (**NSF**), ($10,970), 2012-2013.

10. Equipment Supplement: An Experimental Setup to Study the Interplay of Error and Power in Organic-Spintronic Memories, **National Science Foundation** (**NSF**), ($40,619), 2012-2013.
11. Research Experience for Teachers (RET) Supplement of **NSF** CAREER Error Power and Reliability for Nano-Silicon and Beyond ($12500), 2010-2014.
12. Research Experience for Undergraduates (REU) Supplement of **NSF** CAREER Error Power and Reliability for Nano-Silicon and Beyond ($12000), 2009-2014.
13. "EMT/Nano: Energy Minimization Computing using Field Coupled Nanomagnets--Modeling and Fabrication", **National Science Foundation (NSF)**, with PI: Sarkar, Co-PI: Bhanja, ($250,000), 2008-2012.
14. "CAREER: Error Power and Reliability for Nano-Silicon and Beyond", **National Science Foundation (NSF)**, Division of Computer and Communication Foundations, PI: Bhanja, ($ 400,000), 2007-2014.
15. "CCLI (Exploratory): Introduction of Nano-computing course module in standard Electrical Engineering Courses", **National Science Foundation (NSF**), PI: Bhanja, Co-PI: Wiley, ($ 145,948), 2008-2011.
16. "CRI: Infrastructure acquisition for sub-100 nano VLSI research", **National Science Foundation (NSF)**, PI: Bhanja, Co-PIs: H. Zheng, S. Katkoori, N. Ranganathan, V.K. Jain, ($ 215,023), 2006-2008.
17. "SGER: Independent Component Analysis on Coarse-grain Reconfigurable VLSI (for sensor analysis and fusion)", **National Science Foundation (NSF)**, PI- Jain and Co-PI- Bhanja, ($40,000), 2004-2006.
18. "Modeling of Switching Activity in Sequential Circuits Using Dynamic Bayesian Networks," New Researcher Award, **University of South Florida**, ($9,200), 2002.

Invited Talks

1. Invited Speaker, "Cellular Automata for Field-Coupled Nanocomputing", CRAW/CDC/NSF workshop on Fostering Diversity in Design Automation, **National Science Foundation**, 2014.
2. Invited Speaker, "Energy Minimum NanoMagnetic Computing For Computer Vision Problems", Workshop on Field Coupled NanoComputing, Sponsored by **National Science Foundation**, 2013.
3. Invited Speaker, Speed Networking Mentor, Design and Automation Young Faculty Workshop (co-sponsored by NSF, ACM SIGDA, IEEE CEDA, SRC and DAC), June 2012.
4. Invited Speaker and Mentor: NSF funded minority student conference NC-LSAMP, North Carolina A&T State University, Greensboro, North Carolina, September 2012.
5. Invited Speaker, "NSF CAREER Proposal: Experiential Perspective", **National Science Foundation** , CISE CAREER Proposal Writing Workshop, 2012.
6. Invited Speaker, "A Review of Magnetic Cellular Automata Systems", **IEEE International Symposium on Circuits and Systems (ISCAS),** 2011.
7. Invited Speaker, "QCAPro - An Error-Power Estimation Tool for QCA Circuit Design", **IEEE International Symposium on Circuits and Systems (ISCAS),** 2011.
8. Invited Speaker, "Probabilistic Macromodeling for QCA Circuits" in **International Workshop on QCA**, UBC, Vancouver, 2009.
9. Invited Speaker, Second DSRC TeraChip workshop, sponsored by **Defense Sciences Research Council** (DSRC), 2008.
10. Invited Speaker, "Field Coupled Nano-Computing" for National Symposium on Emerging Computing, **IEEE W**omen in Engineering, India, 2007.

In The News

1. Nanoscale magnets could compute complex functions significantly faster than conventional computers- National Science Foundation, News from the Field, October, 2015. http://www.nsf.gov/news/news_summ.jsp?cntn_id=136758&org=NSF.
2. Featured in National Science Foundation front-page Slider, http://myweb.usf.edu/~bhanja/
3. USF team finds new way of computing with interaction-dependent state change of nanomagnets, http://www.eurekalert.org/pub_releases/2015-10/uosf-utf102815.php
4. Study finds new way of computing with interaction-dependent state change of nanomagnets, http://phys.org/news/2015-10-interaction-dependent-state-nanomagnets.html
5. Press Release, Nanotechnology Now-- http://www.nanotech-now.com/news.cgi?story_id=52474
6. Nanomagnets able to solve complex functions significantly faster than conventional computers; Read more at DEEPSTUFF.ORG-- http://www.deepstuff.org/nanomagnets-able-to-solve-complex-functions-significantly-faster-than-conventional-computers/
7. Team Finds New Way of Computing with Interaction-Dependent State Change of Nanomagnets--https://scicasts.com/scientific-computing/1864-nanotechnology/10225-team-finds-new-way-of-computing-with-interaction-dependent-state-change-of-nanomagnets/
8. Featured Engineer in Electrical Engineering Community, EEWeb, eeweb.com (http://www.eeweb.com/spotlight/interview-with-dr.-sanjukta-bhanja), February 2015.
9. In Computing Research Association-Women (CRA-W) Newsletter http://cra-w.org/Portals/0/Pdfs/summerfall14_web-2.pdf, 2014.
10. USF teams receive grants to develop socially beneficial products, http://www.83degreesmedia.com/innovationnews/NSF120214.aspx, Dec 2014.